WHAT IS CLAIMED IS:

1. A method of individually packaging devices formed on a wafer with a cover wafer comprising the steps of:

providing a plurality of devices formed on a wafer substrate having a selected size;

providing an interposer wafer having substantially said selected size and defining a plurality of open areas separated by a first plurality of parallel and spaced apart grid members intersecting a second plurality of parallel and spaced apart grid members, said interposer wafer having a top side and a substrate side and a selected thickness;

bonding a top wafer having substantially said selected size to said top side of said first and second pluralities of intersecting grid members of said interposer wafer to form a cover wafer structure comprising said bonded top wafer and said interposer wafer defining individual device areas;

bonding said substrate side of said interposer wafer to said wafer substrate to provide a seal around the perimeter of selected ones of said plurality of devices between parallel pairs of intersection grid members and under said top wafer; and

cutting through said top wafer and said intersecting grid member of said interposer wafer to provide separation between individual ones of said sealed devices.

2. The method of claim 1 further comprising the steps of sawing two parallel saw kerfs into the substrate side of said first and second pluralities and partially through said selected thickness to leave an uncut top portion prior to said step of bonding said cover wafer structure to said wafer structure.

3. The method of claim 1 wherein said top wafer is transparent such that said defined individual device areas are individual window areas.

4. The method of claim 3 wherein said plurality of devices are MEMS devices.

5. The method of claim 4 wherein said plurality of MEMS devices are DMD™ spatial light modulators.

6. The method of claim 3 further comprising the step of defining said transparent window areas by forming an aperture mask of intersecting dark lines on said transparent top wafer.

7. The method of claim 6 wherein said first and second pluralities of parallel intersecting grid members are in register with said intersecting dark lines on said transparent top wafer.

8. The method of claim 1 further comprising the step of applying a strip of getter material on at least one of the sides of said grid members of said interposer wafer such that each sealed device includes at least one strip of said getter material in the sealed space.

9. The method of claim 2 wherein said step of cutting comprises the step of sawing pairs of saw kerfs through said window wafer and through the uncut top portion of said intersecting grid members and wherein said saw kerfs are in register with said two parallel saw kerfs in said substrate side of said interposer wafer.

10. The method of claim 1 wherein said interposer wafer has a thickness of between about 0.5 mm to about 1.1 mm.

11. The method of claim 1 wherein said top wafer has a thickness of between about 0.7 mm and about 3 mm.

12. The method of claim 1 further comprising the steps of passivating the interior of said device prior to fully sealing said device.

13. The method of claim 1 further comprising the step of breaking said wafer substrate with said sealed MEMS device at said saw kerfs to divide said MEMS device into sealed and individual units.

14. The method of claim 13 further comprising the steps of encapsulating the sides of said sealed individual devices to provide additional support and protection.

15. A wafer structure defining a multiplicity of devices individually sealed by a cover wafer comprising:

a substrate wafer having a selected size and including said multiplicity of devices formed thereon;

an interposer wafer with a top side and a substrate side and having substantially said selected size, said substrate side bonded to said substrate wafer and said interposer wafer comprising a first plurality of parallel and spaced apart grid members and a second plurality of parallel and spaced apart grid members intersecting said first plurality of grid members to define a multiplicity of open areas in register with said multiplicity of devices formed on said substrate wafer; and

a top wafer having a top surface and a bottom surface and substantially said selected size and said bottom surface bonding to said top side of said interposer wafer so as to provide a seal

along the perimeter of selected ones of said multiplicity of devices between parallel pairs of intersecting grid members and under said top wafer, said top wafer further defining kerfs cut through said top surface of said top wafer and said intersecting grid members of said interposer wafer to provide separation between individual ones of said sealed devices.

16. The wafer structure of claim 15 wherein said kerfs comprise a parallel pair of spaced kerfs.

17. The wafer structure of claim 16 wherein said substrate side of said grid member defines a parallel pair of spaced kerfs, and said kerfs defined in said top surface of said top wafer in register with said parallel kerfs defined in said substrate side of said grid members.

18. The wafer structure of claim 15 wherein said multiplicity of devices are MEMS devices.

19. The wafer structure of claim 18 wherein said multiplicity of MEMS devices are DMD™ spatial light modulators.

20. The wafer structure of claim 15 wherein said top wafer is transparent.

21. The wafer structure of claim 20 wherein said top wafer further comprises a non-transparent aperture mask comprised of intersecting dark lines formed on said transparent wafer to define said window areas.

22. The wafer structure of claim 21 wherein said first and second intersecting grid members are in register with said intersecting dark lines on said transparent wafer.

23. The wafer structure of claim 15 further comprising getter material on the sidewalls of said grid members of said interposer wafer such that each sealed device includes at least one portion of getter material in the sealed space.

24. The wafer structure of claim 15 wherein said interposer wafer has a thickness of between about 0.5 mm and about 1.1 mm.

25. The wafer structure of claim 15 wherein said top wafer has a thickness of between about 0.7 mm and about 3 mm.